Amendments to the Specification

Please replace the paragraph at page 24, lines 14-19 with the following amended paragraph:

Figure 10 illustrates a second method of increasing processing power is by connecting more than one chassis together in a daisy chain or similar arrangement. Concerning the "daisy chain" inputs ~~170~~, Figure 10 also illustrates how a similar effect can be achieved using the unmodified apparatus (Figure 3), providing the apparatus is not monitoring its full complement of bearer signals. The external inputs ~~140~~ can thus be connected to the external outputs 85 of the previous chassis, instead of using special inputs 170 as shown in Figures 7 and 8.

Please replace the paragraph at page 38, lines 24-29 with the following amended paragraph:

Data is transferred into the SBC memory using cPCI DMA transfers to a data buffer 380. This ensures the very high data throughput that may be required if large amounts of data are being stored. The main limitation in the amount of data that is processed will be due to the applications software that processes it. It is therefore the responsibility of the Packet Processor 150 to carry out as much pre-processing of the data as possible so that only that data which is relevant is passed up into the application domain.